



PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Hou, et al.
Appl. No.	:	10/600,377
Filed	:	June 20, 2003
For	:	Method of etching uniform silicon layer
Examiner	:	DEO, DUY VU NGUYEN
Group Art Unit	:	1765

DECLARATION OF PAUL YIH

United States Patent and Trademark Office  
P.O. Box 1450  
Arlington, VA 22313-1450

Dear Sir:

I, Paul Yih (*Email: paulyih@auo.com, Cellular: 0968-377-926 (Taiwan)*), declare as follows:

1. I have completed a B.S. of Electronics Engineering, minor in Computer Science, at the National Chiao-Tung University of Taiwan in 1988 (GPA: 3.8/4.0) and I have obtained an Electrical Engineering Ph.D. in Microelectronics from the University of Cincinnati, Cincinnati, OH in 1994 (GPA: 3.8/4.0). My thesis related to a "Reactive Ion Etching of Crystalline Silicon Carbide and Fabrication of Silicon Carbide Devices", and I have been involved in Research Assistance for the University of Cincinnati concerning:

- RIE and ECR of Si, SiO<sub>2</sub>, and c-SiC in CHF<sub>3</sub>, CF<sub>4</sub>, SF<sub>6</sub>, NF<sub>3</sub> with O<sub>2</sub> / H<sub>2</sub> plasmas
- RIE and ECR of Si, SiO<sub>2</sub>, and c-SiC in CHF<sub>3</sub>/CF<sub>4</sub>, CHF<sub>3</sub>/SF<sub>6</sub>, CHF<sub>3</sub>/NF<sub>3</sub> plasmas
- Metal contact: Ti, W, Ta, Ni, Al, and ITO on c-SiC
- Devices Fabrication: SiC/Si HBT, Blue LED, c-SiC high breakdown diode
- Selective growth planar and blanket planar heterodiode

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I have worked two years doing research at the Display Research Department of the Bell Laboratory of AT&T, Murray Hill, NJ, four years as an integration engineer at the VLSI Technology Department of the Bell Laboratory of Lucent Technology, Orlando, FL., and I am currently working as Process Manager in ACM Research, a Venture capital founded startup, Fremont, CA.

I authored 20 publications and am an inventor in 8 patents.

2. I am familiar with the prosecution of the present application, including the Office Action mailed January 11, 2006 and the references cited therein.

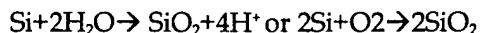
3. I understand that pending Claims 1-3, 5-10, 12-15 and 17-20 have been rejected as obvious over US 6,204,130 to Gardner (hereinafter "Gardner") in view of the admitted prior art.

I understand that Gardner is deemed by the U.S. Patent Examiner to teach treating a silicon layer using a gas comprising oxygen and an etching agent, and in particular "forming an oxide layer (claimed etching buffer layer) by oxygen treatment and H<sub>2</sub>O (claimed etching agent) (col. 4, lines 34-43)".

I note that col. 4, lines 34-43 of Gardner recites "*The polysilicon block 209 is oxidized in an oxygen bearing ambient (e.g., O<sub>2</sub> and or H<sub>2</sub>O). The oxidation generally forms an oxide layer 211 on exposed surfaces of the polysilicon block 209 by consuming a portion of the polysilicon block 209. The resultant structure is depicted in Fig. 2E. The oxidation of the polysilicon block 209 may be performed using a number of different known oxidation techniques including, for example, thermal oxidation. As will be discussed below, the remaining portion 210 of the polysilicon block 209 is used as a gate electrode*".

I note in particular that the recitation that the "*polysilicon block 209 is oxidized in an oxygen bearing ambient (e.g., O<sub>2</sub> and or H<sub>2</sub>O)*" means that the gas existing in the "oxygen bearing ambient" functions as an oxidant reacting with the polysilicon block 209 according to one of the following chemical formulae.

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I note that the above excerpt describes without doubt both  $\text{O}^2$  and  $\text{H}_2\text{O}$  as an "oxygen bearing ambient" for oxidizing the polysilicon block, not as an etching agent.

3. I find no suggestion in Gardner that  $\text{H}_2\text{O}$  can be considered as an "etching agent" for the polysilicon block.

I further note that to the extent of my knowledge,  $\text{H}_2\text{O}$  is typically used in the field of semiconductor process as a solvent or as a source for providing O or H atoms.  $\text{H}_2\text{O}$  is not, to the extent of my knowledge, used as an "etching agent" in the field of semiconductor process.

4. In view of the above, I submit that Gardner, and in particular col. 4, lines 34-43 of Gardner, does not teach or suggest treating a silicon layer using a gas comprising oxygen and an etching agent.

5. I declare that all statements made herein are true, and that all statements made upon information and belief are believed to be true, and further, that these statements were made with the knowledge that willful, false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. § 1001, and that willful, false statements may jeopardize the validity of the application, or any patent issuing thereon.

Dated: 6-2-2006

By: Paul YIH  
Dr. Paul YIH